

1        CLAIMS

2        What is claimed is:

3        1.        A field-enhanced MIS / MIM electron emitter device, comprising:  
4                an electron supply structure;  
5                at least one protrusion formed on a top surface of said electron supply structure;  
6                an insulator formed above said electron supply structure and said at least one  
7                protrusion; and  
8                a top conductive layer formed on said insulator.

9  
10        2.        The device of claim 1, wherein said electron supply structure comprises a  
11                conductive substrate.

12  
13        3.        The device of claim 1, wherein said electron supply structure further  
14                comprises:  
15                an electron supply layer formed above said conductive substrate.

16  
17        4.        The device of claim 3, wherein said electron supply layer is formed from  
18                one of a doped and an undoped semiconductor.

19  
20        5.        The device of claim 4, wherein said doped semiconductor is a doped  
21                polysilicon and said undoped semiconductor is an undoped polysilicon.

22  
23        6.        The device of claim 4, wherein for said doped semiconductor, selected  
24                areas of said doped semiconductor are doped.

25

1        7.     The device of claim 4, wherein for said doped semiconductor, a doping  
2 level of said doped semiconductor varies in a depth direction.

3

4        8.     The device of claim 1, wherein said insulator is substantially conformal to  
5 said electron supply structure including said at least one protrusion.

6

7        9.     The device of claim 1, wherein said insulator is relatively thinner near said  
8 at least one protrusion compared to flat regions of said electron supply structure.

9

10       10.    The device of claim 9, wherein said insulator has a substantially flat top  
11 surface or said insulator has an hourglass shape local to said at least one protrusion.

12

13       11.    The device of claim 1, wherein said insulator is formed from at least one  
14 of diamond-like carbon and oxides, nitrides, carbides, and oxynitrides of silicon,  
15 aluminum, titanium, tantalum, tungsten, hafnium, zirconium, vanadium, niobium,  
16 molybdenum, chromium, yttrium, scandium, nickel, cobalt, beryllium, and magnesium.

17

18       12.    The device of claim 2, wherein said conductive substrate is formed from at  
19 least one of metal, doped polysilicon, doped silicon, graphite, a metal coating on glass, a  
20 metal coating on ceramic, a metal coating on plastic, an ITO coating on glass, an ITO  
21 coating on ceramic, and an ITO coating on plastic.

22

23       13.    The device of claim 12, wherein said metal or said metal coating includes  
24 at least one of aluminum, tungsten, titanium, copper, gold, tantalum, platinum, iridium,  
25 palladium, rhodium, chromium, magnesium, scandium, yttrium, vanadium, zirconium,

1 niobium, molybdenum, silicon, beryllium, hafnium, silver, and osmium and alloys and  
2 multilayered films thereof.

3

4 14. The device of claim 12 wherein at least one of said metal coating and said  
5 ITO coating is patterned.

6

7 15. The device of claim 1, wherein said top conductive layer is formed from at  
8 least one of a metal, doped polysilicon, graphite, and alloys, and multilayered films  
9 thereof.

10

11 16. The device of claim 15, wherein said metal includes at least one of  
12 aluminum, tungsten, titanium, molybdenum titanium, copper, gold, silver, tantalum,  
13 platinum, iridium, palladium, rhodium, chromium, magnesium, scandium, yttrium,  
14 vanadium, zirconium, niobium, molybdenum, hafnium, silver, and osmium and any alloys  
15 and multilayered films thereof.

16

17 17. The device of claim 1, wherein said top conductive layer is patterned.

18

19 18. A method of fabricating a field-enhanced MIS/MIM electron emitter  
20 device, comprising:

21 forming an electron supply structure;

22 forming at least one protrusion on a top side of said electron supply structure;

23 forming an insulator on said electron supply structure and said at least one  
24 protrusion; and

25 forming a top conductive layer on said insulator.

1

2        19.    The method of claim 18, wherein said step of forming said electron supply  
3 structure includes:

4                forming a conductive substrate.

5

6        20.    The method of claim 19, wherein said step of forming said electron supply  
7 structure includes:

8                forming an electron supply layer above said conductive substrate.

9

10       21.    The method of claim 20, wherein said electron supply layer is formed from  
11 one of a doped and an undoped semiconductor.

12

13       22.    The method of claim 21, wherein said doped semiconductor is a doped  
14 polysilicon and said undoped semiconductor is an undoped polysilicon.

15

16       23.    The method of claim 21, wherein said forming said doped semiconductor  
17 includes:

18                doping said semiconductor in selected areas.

19

20       24.    The method of claim 21, wherein forming said doped semiconductor  
21 includes:

22                varying a doping level in a depth direction.

23

1           25. The method of claim of 22, wherein said step of forming said polysilicon  
2 includes:

3           depositing said polysilicon by at least one of LPCVD, PVD, PECVD and other  
4 CVD variants.

5

6           26. The method of claim 22, wherein said step of forming said insulator  
7 includes:

8           oxidizing said polysilicon and said at least one protrusion thereon.

9

10          27. The method of claim 26, wherein oxidizing step includes:

11          oxidizing said polysilicon and said at least one protrusion thereon by at least one  
12 of plasma oxidation, wet thermal oxidation, dry thermal oxidation, and electrochemical  
13 oxidation.

14

15          28. The method of claim 18, wherein said step of forming said insulator  
16 includes:

17          forming said insulator such that said insulator is relatively thinner near said at  
18 least one protrusion compared to a flat region of said electron supply layer.

19

20          29. The method of claim 28, wherein step of forming said insulator further  
21 includes:

22          forming said insulator such that a top of said insulator is substantially flat.

23

1           30. The method of claim 28, wherein step of forming said insulator further  
2 includes:

3           forming said insulator such that said insulator has an hourglass shape local to said  
4 at least one protrusion.

5

6           31. The method of claim 18, wherein said insulator is formed from at least one  
7 of a diamond-like carbon, oxides, nitrides, carbides and oxynitrides of silicon, aluminum,  
8 titanium, tantalum, tungsten, hafnium, zirconium, vanadium, niobium, molybdenum,  
9 chromium, yttrium, scandium, nickel, cobalt, beryllium, magnesium, and combinations  
10 thereof.

11

12           32. The method of claim 19, wherein said conductive substrate is formed from  
13 at least one of a metal, doped polysilicon, doped silicon, graphite, a metal coating on  
14 glass, a metal coating on ceramic, a metal coating on plastic, an ITO coating on glass, an  
15 ITO coating on ceramic, an ITO coating on plastic, and combinations thereof.

16

17           33. The method of claim 32, wherein said metal or metal coating includes at  
18 least one of aluminum, tungsten, titanium, copper, gold, tantalum, platinum, iridium,  
19 palladium, rhodium, chromium, magnesium, scandium, yttrium, vanadium, zirconium,  
20 niobium, molybdenum, silicon, beryllium, hafnium, silver, and osmium and any alloys,  
21 and multilayered films thereof.

22

23           34. The method of claim 32, wherein said step of forming said conductive  
24 substrate includes:

25           patterning at least one of said metal coating and said ITO coating.

1

2       35.    The method of claim 18, wherein said top conductive layer is formed from  
3    at least one of a metal, doped polysilicon, graphite, and alloys or multilayered films  
4    thereof.

5

6       36.    The method of claim 35, wherein said metal includes at least one of  
7    aluminum, tungsten, titanium, molybdenum titanium, copper, gold, silver, tantalum,  
8    platinum, iridium, palladium, rhodium, chromium, magnesium, scandium, yttrium,  
9    vanadium, zirconium, niobium, molybdenum, hafnium, silver, and osmium and any alloys  
10   and multilayered films thereof.

11

12       37.    The method of claim 18, wherein said forming said top conductor  
13    comprises:

14            patterning said top conductor.

15